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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,699	07/29/2004	Somasekar JAYARAMAN	TI-37107	4698

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EXAMINER	
PARIHAR, SUCHIN	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,699	JAYARAMAN ET AL.	
	Examiner	Art Unit	
	Suchin Parihar	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This application 10/710,699 has been examined. Claims 1-12 are pending.

Specification

1. The disclosure is objected to because of the following informalities: The specification is missing the following sections: Brief summary of the invention. Appropriate correction is required.

2. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.

(b) CROSS-REFERENCE TO RELATED APPLICATIONS.

(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.

(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT

(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC

(See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or

REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)

(f) BACKGROUND OF THE INVENTION.

(1) Field of the Invention.

(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.

(g) BRIEF SUMMARY OF THE INVENTION.

(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).

(i) DETAILED DESCRIPTION OF THE INVENTION.

(j) CLAIM OR CLAIMS (commencing on a separate sheet).

(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).

(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Objections

3. Claim 5 is objected to because of the following informalities: The claim recites the limitation "said first cell" beginning on line 6 of the claim. There is insufficient antecedent basis for this limitation in the claim. It is recommended that the word "first" be deleted. Appropriate correction is required.

4. Claim 11 is objected to because of the following informalities: The claim recites the limitation "said first cell" beginning on line 10 of the claim. There is insufficient antecedent basis for this limitation in the claim. It is recommended that the word "first" be deleted. Appropriate correction is required.

5. Claim 6 is objected to because of the following informalities: The meaning of the term "characterized", found on line 8 of claim 6, lacks clarity within the specification. Appropriate correction is required.

6. Claim 5 is objected to because of the following informalities: The intended meaning of the following preamble recitation is unclear: "characterizing a load offered by a cell on an input pin". Examiner suggests the applicant re-phrase said recitation such that its intended meaning is clear. Appropriate correction is required.

7. Claim 12 is objected to because of the following informalities: The meaning of the term "characterized", found on line 9 of claim 12, lacks clarity within the specification. Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

9. **Claims 1, 2, 7 and 8 are rejected under 35 U.S.C. 102(b)** as being anticipated by Salem et al. (5,636,130).

10. With respect to claims 1 and 7, Salem teaches a method and a machine readable medium carrying one or more sequences of instructions to determine whether an integrated circuit operates at a clock speed (Col 1, lines 12-28, i.e. determining design's clock speed), said integrated circuit comprising a combinatorial element, wherein execution of said one or more sequences of instructions (Col 6, lines 42-49, i.e. sequences of instructions) by one more processors contained in said system causes said one or more processors to perform the actions of, and said method comprising: determining a load offered by said combinatorial element when an output path of said

combinatorial element switches in response to a vector provided as an input to said combinatorial element (Col 4, lines 1-10 and Col 1, lines 60-66, i.e. determining the load associated with the selected gate, wherein gate switches states in response to a signal change on its input, Note: a state-switch on a combinatorial element [i.e. gate] may or may not cause a change on the output path); and performing a timing analysis of said integrated circuit by associating said load to a prior element driving said combinatorial element (Col 3, lines 20-38, and Col 2, lines 25-43, i.e. discussion of timing analyzer),(also see Col 7, lines 37-40, i.e. the load associated).

11. With respect to claims 2 and 8, Salem teaches all the elements of claims 1 and 7, from which the claims depend. Salem teaches: determining another load offered by said combinatorial element when an output path of said combinatorial element does not switch in response to a vector provided as an input to said combinatorial element (Col 4, lines 1-10 and Col 1, lines 60-66, i.e. determining the load associated with the selected gate, wherein gate switches states in response to a signal change on its input, Note: a state-switch on a combinatorial element [i.e. gate] may or may not cause a change on the output path); and performing another timing analysis of said integrated circuit by associating said another load to said prior element (Col 3, lines 20-38, and Col 2, lines 25-43, i.e. discussion of timing analyzer, wherein load and input rise time are in association, and input rise time is associated with a gate immediately preceding the gate under consideration).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. **Claims 3, 4, 9 and 10 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Salem et al. (5,636,130) in view of Sun et al. (US PG Pub 2005/0268263).

14. With respect to claims 3 and 9, Salem teaches all the elements of claims 2 and 8, from which the claims depend respectively. Salem does not teach: said timing analysis is performed when said integrated circuit is being analyzed for hold time violations of sequential elements contained in said integrated circuit. However, Sun teaches: said timing analysis is performed when said integrated circuit is being analyzed for hold time violations of sequential elements contained in said integrated circuit (pg 1, paragraph [0010] and pg 2, paragraph [0030], i.e. in order to fix hold time violations of sequential circuit cells, timing analysis is performed on the circuit design). It would have been obvious to one of ordinary skill in the art to incorporate Sun into the invention of Salem because Sun improves the invention of Salem by giving consideration to hold time and setup time violations that may be created by gate propagation delays that are either too short or too long (see pg 1, paragraph [0006]).

15. With respect to claims 4 and 10, Salem teaches all the elements of claims 2 and 8, from which the claims depend respectively. Salem does not teach: said timing analysis is performed when said integrated circuit is being analyzed for setup time violations of sequential elements contained in said integrated circuit. However, Sun teaches: said timing analysis is performed when said integrated circuit is being analyzed for setup time violations of sequential elements contained in said integrated circuit (pg 1, paragraph [0006], i.e. violation of setup time requirements for sequential cells). It would have been obvious to one of ordinary skill in the art to incorporate Sun into the invention of Salem because Sun improves the invention of Salem by giving consideration to hold time and setup time violations that may be created by gate propagation delays that are either too short or too long (see pg 1, paragraph [0006]).

16. **Claims 5, 6, 11 and 12 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Salem et al. (5,636,130) in view of Sun et al. (US PG Pub 2005/0268263) and in further view of Van Brunt (4,527,249).

17. With respect to claims 5 and 11, Salem teaches a method for characterizing a load offered by a cell on an input pin, wherein said cell is contained in a library, said method, and machine readable medium comprising: measuring a capacitance of said pin when said pin when said first set of input vectors are applied to said combinatorial element (Col 4, lines 1-6, i.e. determine the load [capacitance] associated with the selected gate –in light of Col 1, lines 60-67, i.e. response to signal change on input pin); and associating said capacitance to said pin if said cell is to be characterized for setup time violation (Col 7, lines 35-40, i.e. discussion of gate capacitance getting so large as

to increase gate's propagation time, which is directly related to setup and hold time violations). Salem does not teach the relationship between a changing propagation time and setup/hold time violations. However, Sun teaches the relationship between a changing propagation time and setup/hold time violations (pg 1, paragraph [0006], i.e. discussion of setup and hold time requirements). Salem in view of Sun does not teach: determining a first set of input vectors that would cause an output path of a combinatorial element to switch, wherein said combinatorial element is contained in said first cell and connected to said input pin. However, Van Brunt teaches: determining a first set of input vectors that would cause an output path of a combinatorial element to switch, wherein said combinatorial element is contained in said first cell and connected to said input pin (Col 9, lines 43-69, i.e. discussion of using a particular gate's input values and assigned truth table to determine whether an output changes). It would have been obvious to one of ordinary skill in the art to incorporate Sun and Van Brunt into the invention of Salem because: Sun improves the invention of Salem by giving consideration to hold time and setup time violations that may be created by gate propagation delays that are either too short or too long (see pg 1, paragraph [0006]); and Van Brunt improves the invention of Salem by providing a method for which to determine which input values cause a gate to switch states in response to a signal change on tine input pin(s) (see Salem, Col 1, lines 60-68, i.e. discussion of switching states, and its relationship to propagation delay).

18. With respect to claims 6 and 12, Salem in view of Sun and in further view of Van Brunt teach all the limitations of the claims from which they depend, respectively.

Salem teaches: measuring a capacitance of said pin when said second set of input vectors are applied to said combinatorial element (); and associating said capacitance to said pin if said cell is to be characterized for hold time violation (Col 7, lines 35-40, i.e. discussion of gate capacitance getting so large as to increase gate's propagation time, which is directly related to setup and hold time violations). Salem does not teach the relationship between a changing propagation time and setup/hold time violations. However, Sun teaches the relationship between a changing propagation time and setup/hold time violations (pg 1, paragraph [0006], i.e. discussion of setup and hold time requirements). Salem in view of Sun does not teach: determining a second set of input vectors that would not cause said output path to switch. However, Van Brunt teaches: determining a second set of input vectors that would not cause said output path to switch (Col 9, lines 43-69, i.e. discussion of using a particular gate's input values and assigned truth table to determine whether an output changes).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 7:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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